7E7084

Roll No. 15EEBEC021

Total No of Pages: 3

7E7084

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. - 2018
Electronics & Communication Engineering
7EC5A VLSI Design

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL

2. NIL

UNIT- I

Q.1 (a) What are different kinds of MOS transistors? Explain the structure and operation of MOS transistor. [8]

(b) The process parameters for an NMOS are - [8]

Oxide thickness = 500 A° , Substrate doping $M_A = 10^{16}/cm^3$, Polysilicon gate doping $M_D = 10^{20}/cm^3$, Oxide interface fixed charge density = $2\times10^{10}/cm^3$. Calculate the threshold voltage V_T.

OR

Q.1 (a) What are the different techniques of CMOS transistor fabrication? Explain one in detail. [8]

(b) Explain "Depletion mode MOSFET". [8]

UNIT- II

Q.2 (a) Write short note on – [8]

(i) Noise Margins

(ii) Pull-up to pull – down ratio for an NMOS inverter.

(b) Design a resistive load inverter with R = 1kΩ such that at V_{OL} = 0.6V. The enhancement type NMOS driver transistor has following parameters : V_{DD} = 5V, V_T = 1V, $\mu_n.C_{ox}$ = 22μ A/V² – [8]

(i) Determine the aspect ratio

(ii) Determine Noise margins NM_L and NM_H.

OR

Q.2 (a) Derive β_n/β_p ratio of CMOS inverter. [10]

(b) The NMOS device with V_t = 0.7V has its source terminal grounded and a 1.3V is applied to gate. The device has $\mu_n.C_{ox}$ = 100 mA/V², W = 10mm, L = 1mm. Find the value of drain current for V_D = 3V. [6]

UNIT- III

Q.3 (a) Realize the following expression using CMOS inverter – [8]

(i) $AB+\overline{A}\,\overline{B}$

(ii) $\overline{A+BC+DE}$

(iii) AB + BC + AC

(iv) A⊙B

(b) What are DRC rules for layout? State any six DRC rules. [8]

OR

Q.3 (a) Draw the layout using Euler path for $y = \overline{(A+BC)(D+E)}$. [8]

(b) Draw latch – up formation in CMOS inverter. [8]

UNIT- IV

Q.4 (a) What is C^2 MOS logic? Draw logic circuit using it. What are advantages of such logic? [8]

(b) Explain the working of SRAM cell and DRAM cell. [8]

OR

Q.4 (a) Explain pre – charge and evaluation logic. [8]

(b) Draw $y = \overline{(AB+C)}$ using Domino logic. [8]

UNIT- V

Q.5 (a) Write VHDL Code for S – R flip flop and D-flip flop. [10]

(b) List the advantages and limitations of VHDL. [6]

OR

Q.5 (a) Write the difference between FPGA and custom design. [8]

(b) Write the difference between first and back end design. [8]
